PRANAV KUMAR

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RESEARCH INTERESTS

Binary security, program instrumentation, vulnerability detection, compiler optimization, computer architecture, FPGA design, hardware-software co-design, safety-critical embedded systems.

SUMMARY

Security researcher specializing in binary analysis and static program instrumentation. Developing FUSE, a formally verified binary instrumentation tool combining memory-safety (ASAN) and coverage-guided fuzzing (AFL++) for accurate vulnerability detection in deployable binaries without source code. Research focuses on novel register liveness analysis for instrumentation overhead reduction and compiler metadata techniques for improving binary disassembly precision. Background in safety-critical embedded systems, FPGA design, and systems optimization.

EDUCATION

Virginia Tech, MS with Thesis in Computer Engineering (GPA: 3.88/4.0) Aug 2024 – May 2026
Thesis: FUSE: Single-Pass Binary Co-Instrumentation for Accurate Vulnerability Detection
Advisors: Prof. Binoy Ravindran (Virginia Tech), Prof. Freek Verbeek (Open University Netherlands)
Committee: Binoy Ravindran (Chair), Freek Verbeek, Kendall Giles
Coursework: Comp. Arch., Multiprocessor Programming, Compiler Optimization, Linux Kernel Programming, Digital Design

UIET, Panjab University, B.E. in Electronics and Communication Engineering May 2016 – Sep 2020

RESEARCH EXPERIENCE

Graduate Student Researcher, SSRG Lab (Prof. Binoy Ravindran) @Virginia Tech Dec 2024 – May 2026

- Developing **FUSE**, a formally verified binary instrumentation tool combining ASAN memory-safety checks with AFL++ fuzzing counters in a single pass for vulnerability detection.
- Designed novel **register liveness analysis** algorithm that eliminates push/pop pairs at **61% of instrumentation sites**, allowing FUSE to sustain 99.3% of native ASAN throughput on real-world fuzzing targets (zlib, libjpeg-turbo, libpng).
- Discovers **3.29× more coverage edges** than source-level AFL instrumentation.
- Achieved **zero false positives** across 19,350 NIST Juliet test cases vs. RetroWrite's two false positives; 89.5% binary rewriting success vs. RetroWrite's 46.3%.
- Collaborating with **Prof. Freek Verbeek** (Open University Netherlands) on binary metadata formats and compiler-assisted binary disassembly for DARPA EBOSS Challenge.
- Integrated multi-repo CI/CD pipeline using GitLab for automated rapid testing and deployment across diverse binary benchmarks.

Embedded Systems Researcher, ARTPARK @IISc Bangalore May 2023 – Jul 2024

- Under supervision of **Prof. Shishir N. Y. Kolathaya**, developed FOC-based BLDC motor drivers for quadruped robot actuators with real-time CAN-FD control firmware.
- Designed safety-critical embedded Linux motor controller firmware with thermal monitoring and fault detection mechanisms for multi-joint robotic systems.
- Improved torque response by 23% through optimization of motor control algorithms and system integration across STM32/TI MCUs.

PUBLICATIONS

"FUSE: Single-Pass Binary Co-Instrumentation for Accurate Vulnerability Detection" Submitted to **CCS 2026** (Under Review)
Pranav Kumar, F. Verbeek, B. Ravindran
Lead author: developed novel register liveness analysis, implemented binary instrumentation framework, conducted comprehensive evaluation across benchmarks

"Adding Compilation Metadata To Binaries To Make Disassembly Decidable" IEEE QRS 2026, Florence, Italy; also presented at **EuroLLVM 2026**, Dublin. arXiv:2604.19628
D. Engel, F. Verbeek, **Pranav Kumar**, B. Ravindran
Key contributor: methodology design and binary format analysis for compiler metadata integration

"Autonomous System of Heavy Vehicle Using CAN Networking" Published at **ICDEMI**, Springer - Nov 2024
Pranav Kumar, Uba. Sunil
Developed during Flux Auto work: decentralized CAN network architectures and autonomous vehicle control systems

SKILLS & TOOLS

Binary Analysis & Instrumentation: Static binary instrumentation, dynamic analysis, binary disassembly/reassembly, control flow graph analysis, dataflow analysis, register liveness analysis, ELF binary format, x86-64 assembly
Fuzzing & Security: AFL++, AddressSanitizer (ASAN), coverage-guided fuzzing, memory safety instrumentation, vulnerability detection, shadow memory analysis
Compilers & Optimization: LLVM, GCC, compiler optimization techniques, register allocation, instruction selection, formally verified disassembly (FoxDec)
Hardware Design: SystemVerilog, FPGA design (Quartus), RISC-V architecture simulation (Chipyard), cache design, performance analysis
Development Tools: Git, GitLab CI/CD, Docker, Linux kernel programming, GDB, debugging, formal methods (binary verification)

GRADUATE COURSEWORK PROJECTS

Register Liveness Analysis for Binary Instrumentation *2025*
- Core thesis contribution: Designed and implemented register liveness analysis algorithm for reducing instrumentation overhead in binary code without source information.

Cache Optimization on RISC-V Architecture, Virginia Tech *Aug 2024 – Dec 2024*
- Evaluated cache replacement policies (LRU, PLRU, random) using Chipyard RISC-V simulator; analyzed performance tradeoffs and memory hierarchy optimization.

Energy-Aware Real-Time Scheduling using Software-Based Frequency Scaling, Virginia Tech *Aug 2024 – Dec 2024*
- Implemented DVFS (Dynamic Voltage and Frequency Scaling) on STM32 RTOS systems for energy-aware real-time task scheduling.

FPGA-Based RTL Design: Road Rage Game on DE1-SoC, Virginia Tech *Jan 2025 – May 2025*
- Developed complete hardware design in SystemVerilog for game logic and joystick interfacing; hands-on FPGA implementation demonstrating real-time hardware control.

Rust Language Memory Reclamation Techniques, Virginia Tech *Aug 2024 – Dec 2024*
- Implemented epoch-based reclamation (EBR) and hazard pointers (HP) in Rust; developed custom allocator and benchmarked performance for concurrent systems.

TEACHING & MENTORING

Graduate Research Assistant, SSRG Lab, Virginia Tech Dec 2024 – May 2026
- Mentored undergraduate researchers on binary analysis and program instrumentation techniques.
- Contributed to research methodology design and documentation for DARPA EBOSS Challenge.

INDUSTRY EXPERIENCE

Embedded Systems Supervisor, VNX Robotics, Vietnam June 2025 – Present
- Supervising low-level system development for quadruped robots using Linux and ROS2 stack.
- Working on real-time performance optimizations to improve quadruped operations by increasing response time by 30%.
- Guiding development of firmware optimization techniques for safety-critical embedded systems and quadruped safety functionality.

Embedded System Engineer, Flux Auto Pvt. Ltd. Jun 2021 – Mar 2023
- Designed decentralized CAN networks and FreeRTOS firmware for real-time autonomous vehicle control (tractors, forklifts, BOPT).
- Developed OBD-II diagnostics, vehicle monitoring, and automotive IC libraries improving control by 40%.
- Led firmware architecture with autonomous modules, reducing development time by 35% and earning three Best Employee awards.

Embedded Firmware Engineer, Futuristic Labs Pvt. Ltd. Jan 2020 – May 2021
- Developed safety-critical firmware for autonomous cooking systems with precise temperature and motor control.
- Implemented FreeRTOS-based multitasking control and RTOS-to-compute communication bridges for system integration.

SELECTED PROJECTS

Stepper_STSPIN220-library | *C++, Arduino IDE, Driver Development* *Dec 2020*
- Generic driver for 1/256 microstepping stepper motor control. Blog Link

e-YRC (IIT Bombay) | *Computer Vision, Embedded Systems, Finite State Machine* *Oct 2018 – Feb 2019*
- Developed line following algorithm using FSM with OpenCV object detection. Video, Code

3D/2D Printer Modular Design | *Marlin, Stepper Motors, Embedded C* *Jan 2017 – May 2017*
- Multipurpose 3-D printing platform with swappable modules for 2D plotting and 3D printing.

ACHIEVEMENTS & FELLOWSHIPS

- 2019 – **ROSCon-19 Scholarship Holder**, Macau, China (selected for excellence in robotics research)
- 2019 – Awardee for excellence in Technology field by **Mrs. Kirron Kher (MP, Chandigarh)**
- 2019 – 1st Award at Design and Idea Competition by IIC, Panjab University

- 2019 – **Mentor** of winning team at **Smart India Hackathon-2019** by Kokuyo Camlin at IIT Hyderabad
- 2019 – **Google Summer of Code (GSoC)**, BeagleBoard.Org on embedded systems and device drivers
- 2018 – Winner of Pocket Beagle at **Mouser electronics** event in **IIT Roorkee**
- 2021-2022 – Three times **Best Employee per Quarter** at Flux Auto

COMMUNITY & VOLUNTEER WORK

- Organized Hackathons for three consecutive years in university
- 2018 & 2019 Speaker at **Software Freedom Day**, Panjab University
- Speaker & Organizer in Embedded Community in Chandigarh Area
- 2018 Volunteer at TECHNOCIAN Championship
- Community Head of Embedded Systems Telegram Group
- Student Lead of College Eyantra Robotics Lab for 2.5 years
- Regular participant of voluntary Blood Donation Camp